ANALOG DEVICES

CPL

ICs FOR LASERS

USING THE AD9661A EVALUATION BOARD

Introduction

The AD9661A evaluation board is comprised of two printed circuit boards. The Laser Diode Driver (LDD) Resource board is both a digital pattern generator and an analog reference generator (see LDD Resource Board Block Diagram). The board is controlled by an IBM compatible personal computer through a standard printer cable. The resource board interfaces to the AD9661A Evaluation Board, which contains the AD9661A, a level shift circuit for the analog input, and a socket for an N type laser diode. A dummy load circuit for the laser diode is included for evaluation. Power for all the boards is provided through the banana jacks on the AD9661A Eval board. These should be connected to a linear, +5V power supply. Schematics for the LDD Resource board, AD9661A Eval board, and Dummy Load are included, along with a bill of material and layout information.

Plugging the boards together

The LDD Resource board and AD9661A Eval board are normally plugged together for shipment. If they become separated for any reason, the user may plug them together. The LDD Resource board sits on top of the AD9661A Eval board; line up the 20 pin headers. Four SMB connectors also plug together once the 20 pin headers are aligned. It is best to have power supplies off during this operation.

PC Requirements

The AD9661A evaluation board requires an IBM compatible personal computer with the following:

1. Windows version 3.1 software.
2. Standard parallel printer port.
3. A Mouse.

The printer cable should be removed from any printer (or other device) and plugged into the Centronics connector on the LDD Resource board (P1) before running any software for the board. The control software will use the LPT1 printer port address by default. To change the address, click the "Change Port Address" button with the mouse and select the appropriate address.

** **Warning** ** Some printer cables may not have all 25 pins connected to the Centronics connector. Such cables should not be used for controlling the LDD Resource board.

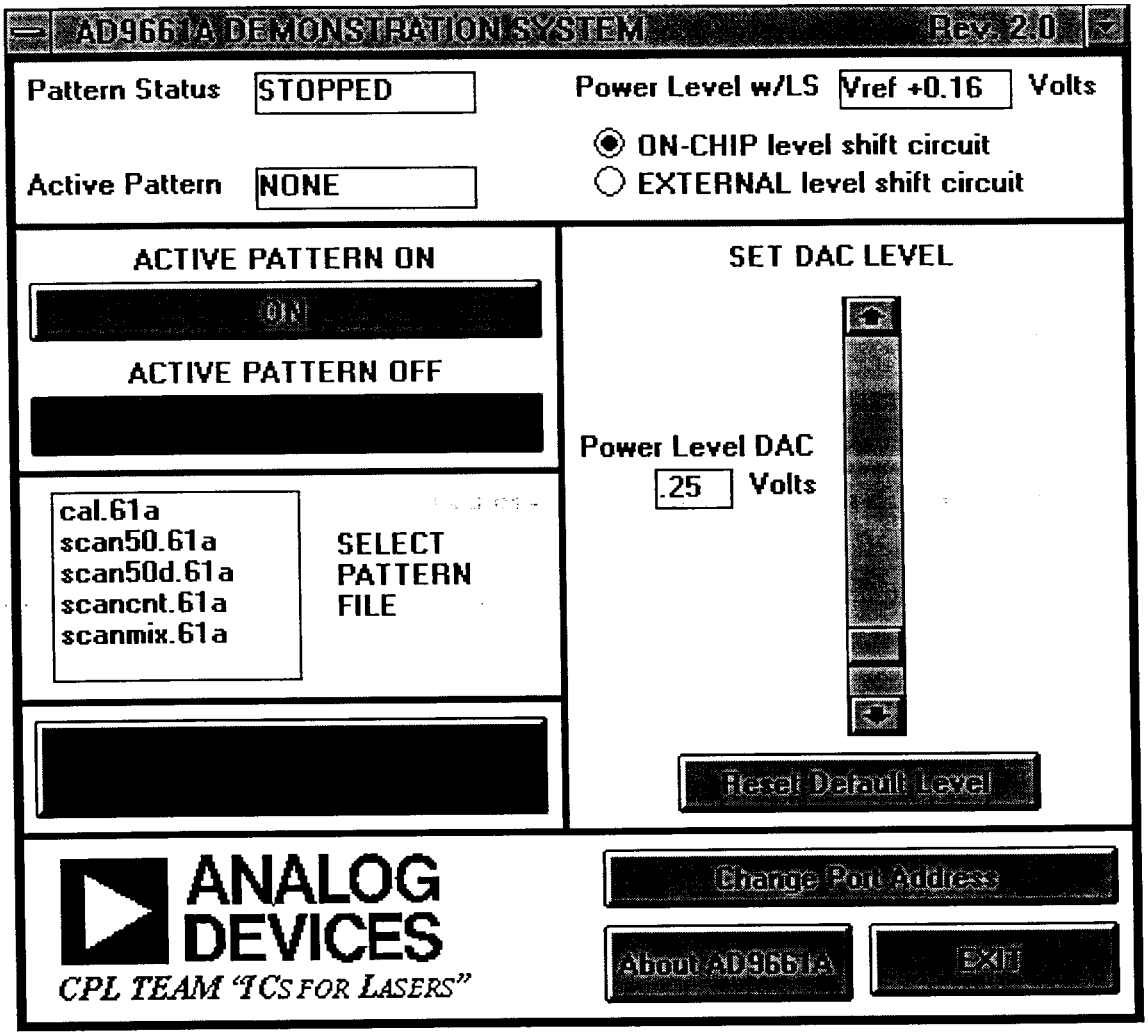
Software Control

The LDD Resource board is controlled through a standard printer cable. Installation of the software is simple. Insert the 3.5" diskette labeled "AD9661A Demo Software" into the PC's floppy disk drive. From the Windows File Manager choose FILE / RUN. In the command line type "B:\SETUP" (assuming the floppy drive is drive B). The software will install the control software on the computer's hard drive, and place a Group called "AD9661A", and an icon called "AD9661A" in Program Manager.

NOTE: The installation software assumes there is a file called "VBRUN300.DLL" in the windows \SYSTEM directory. If there is not, the installation software will generate an error message and terminate. If this occurs, copy the file from the "AD9661A Demo Software" floppy into the windows \system directory. The software should then install properly.

Once the software is installed on the hard drive, double click the AD9661A icon to start the control software. The LDD Resource boards and the AD9661A Eval board should be attached to the PC's printer cable and the power supply to the AD9661A Eval board (+5V) active before the software is initiated. When the software is running, all commands are mouse driven.

The analog reference circuit on the LDD Resource Board provides two buffered 8 bit DACs. The two DACs provide two ways to set the voltage at the 9661A POWER LEVEL pin. When assembled, the board is configured to drive POWER LEVEL with the 9661A's on-board level shift circuit. The DAC output (0V to 2.55V) is attenuated by resistors to the range (0 to 1.6V). This voltage is applied to LEVEL SHIFT IN (pin 4). The 9661A adds V_{REF} to $V_{LEVEL\ SHIFT\ IN}$, so that $V_{LEVEL\ SHIFT\ OUT} = (V_{LEVEL\ SHIFT\ IN} + V_{REF})$. Since LEVEL SHIFT OUT is tied to POWER LEVEL, this gives $V_{POWER\ LEVEL}$ in the range 'V_{REF}' to 'V_{REF} + 1.6V'.



AD9661A Evaluation Board Control Software

In this configuration, the wire-hole labeled "LOUT" is tied to the wire-hole "PLEV". The external op-amp (U2) and associated components (R10 - R13, C5) are unnecessary. When the demonstration software is launched, the DAC output is set to 0.25V (which provides a $V_{POWER\ LEVEL}$ of 0.16V). The user may adjust the DAC voltage up or down by clicking the arrows on the scroll bar.

The evaluation board may be altered so that an external op-amp circuit drives POWER LEVEL (pin 12). The op-amp circuit is functionally the same as the on-chip level shift described above: given a voltage in the range (0 to 1.6V), its output ranges from (V_{REF} to V_{REF} + 1.6V). When using the external level shift, the 9661A's on-board level shift circuit is not used.

To drive POWER LEVEL with the external op-amp, make the following modifications:

1) Cut or remove the wire connecting the wire-holes LOUT and PLEV.

2) Connect the wire-hole OPOUT to PLEV.

3) Install the following components: U2, C5, R10-R13. See the schematic for details. Use ADOP191 or similar op-amp for U2.

After launching the demonstration software, the user must select the second DAC by clicking on the small square check box labeled "EXTERNAL level shift circuit". A warning will appear, telling the user about the required modifications. Click "OK" to continue.

The digital pattern generator copies patterns (from files named *.61A) into the 32K x 16 SRAM memory, and reads them out to the Eval board's interface for the AD9661A's DISABLE, $\overline{\text{CAL}}$, PULSE1 and $\overline{\text{PULSE2}}$ pin connections. The PULSE1 pattern's pulse width is modulated on the LDD Resource Board by the AD9560. Contact Applications Engineering for more information.

The pattern generator can store patterns of up to 800µs with the on board 40MHz clock providing 25ns intervals. All signals have a minimum pulse width of 25ns (one clock period), except PULSE1, whose pulse width is controlled by the AD9560, and may be as low as 2ns.

Six standard patterns are shipped with the software for evaluation. They are:

1. SCAN50.61A
2. SCAN50D.61A
3. SCANP2D.61A
4. SCANMIX.61A
5. SCANCNT.61A
6. CAL.61A

CAL.61A is a static pattern with $\overline{\text{CAL}}$ and DISABLE LOW, and with PULSE1 and $\overline{\text{PULSE2}}$ high. It is intended to allow the user to measure output power from a laser diode, or to adjust the feedback resistor of the AD9661A (see below). All other patterns are dynamic, and are documented on pages x-x. Loading the patterns is done by clicking the mouse on one of the file names in the "PATTERN SELECTION MENU". This will bring up a new dialog box prompting the user to verify the selection. This list will contain the six patterns discussed above, along with any custom patterns added to the software. Custom patterns should be requested through Applications Engineering, and are usually generated within 24 hours of a request.

Once a pattern is selected, the software will load the SRAM; this may take several minutes depending on the size of the pattern and speed of the PC. The software will also verify the pattern to detect errors, if errors cannot be corrected by the software, a message box will prompt the user to contact Applications Engineering. The user should check that the port address is correct, the printer cable is connected, and that the power supply is on as these are the most frequent problems in loading patterns.

When the control software is first run, the LDD Resource board keeps the control signals in a safe state:

DISABLE = HIGH
PULSE1 = LOW
$\overline{\text{PULSE2}}$ = HIGH
$\overline{\text{CAL}}$ = HIGH

This state remains until a pattern is loaded and initiated by the user clicking the mouse in the "ON" button. The pattern stored in memory is repeated until the user clicks the mouse in the "OFF" button, when the control signals are returned to the safe state.

Laser Safe State

The user may disable the pattern generator to the safe state described above, and return the Power Level DAC levels to 0.25V by clicking the mouse on the "LASER OFF" button.

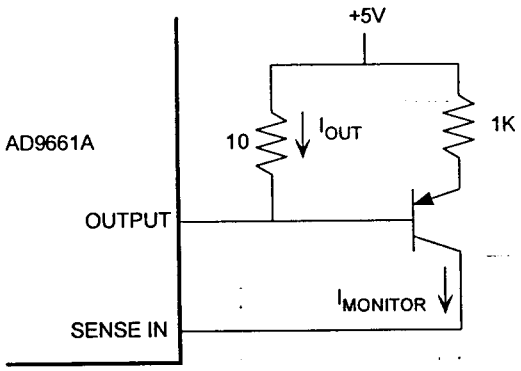
Adjusting the AD9661A's Feedback resistor, R_{GAIN}

The AD9661A Eval boards are built with a fixed R_{GAIN} of 1KΩ (component R3). Alternatively, the Eval board can be modified to allow an adjustable R_{GAIN}. Users wishing to install an adjustable R_{GAIN} should contact Applications Engineering for additional assistance.

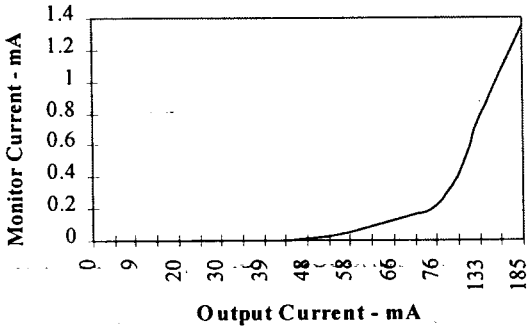
AC performance characterization

Once the software is running, the user may observe the ac switching characteristics of the AD9661A by probing the output directly when using the dummy load circuit. The TRIGGER output (J2) of the LDD Resource board is helpful in triggering the waveform on an oscilloscope. Laser performance can be characterized by replacing the dummy load with an N type laser, and capturing the laser's light output with a fast external photodiode. Contact applications engineering for more information.

AD9661A DUMMY LOAD CIRCUIT



Dummy Load Transfer Function



Connecting other control signals

The AD9661A Eval board may be unplugged from the LDD Resource board and used independently. SMB cables and ribbon cables are available from applications engineering. Users should review the schematics of the AD9661A Eval board and the AD9661A preliminary data sheet before interfacing the board to other control signals.

"ABOUT AD9661A"

Selecting the "ABOUT AD9661A" button will bring up a window with applications information (how to contact Applications Engineering , etc) and a pinout of the AD9661A.

Contacting Applications Engineering

Applications Information is gladly provided by contacting the following:

David Buchanan

email:
DAVID.BUCHANAN@ANALOG.COM

Phone: 910 - 605 - 4252

Fax: 910 - 605 4332

or

David Tesh

email:
DAVID.TESH@ANALOG.COM

Phone: 910 - 605 - 4302

Fax: 910 - 605 - 4332

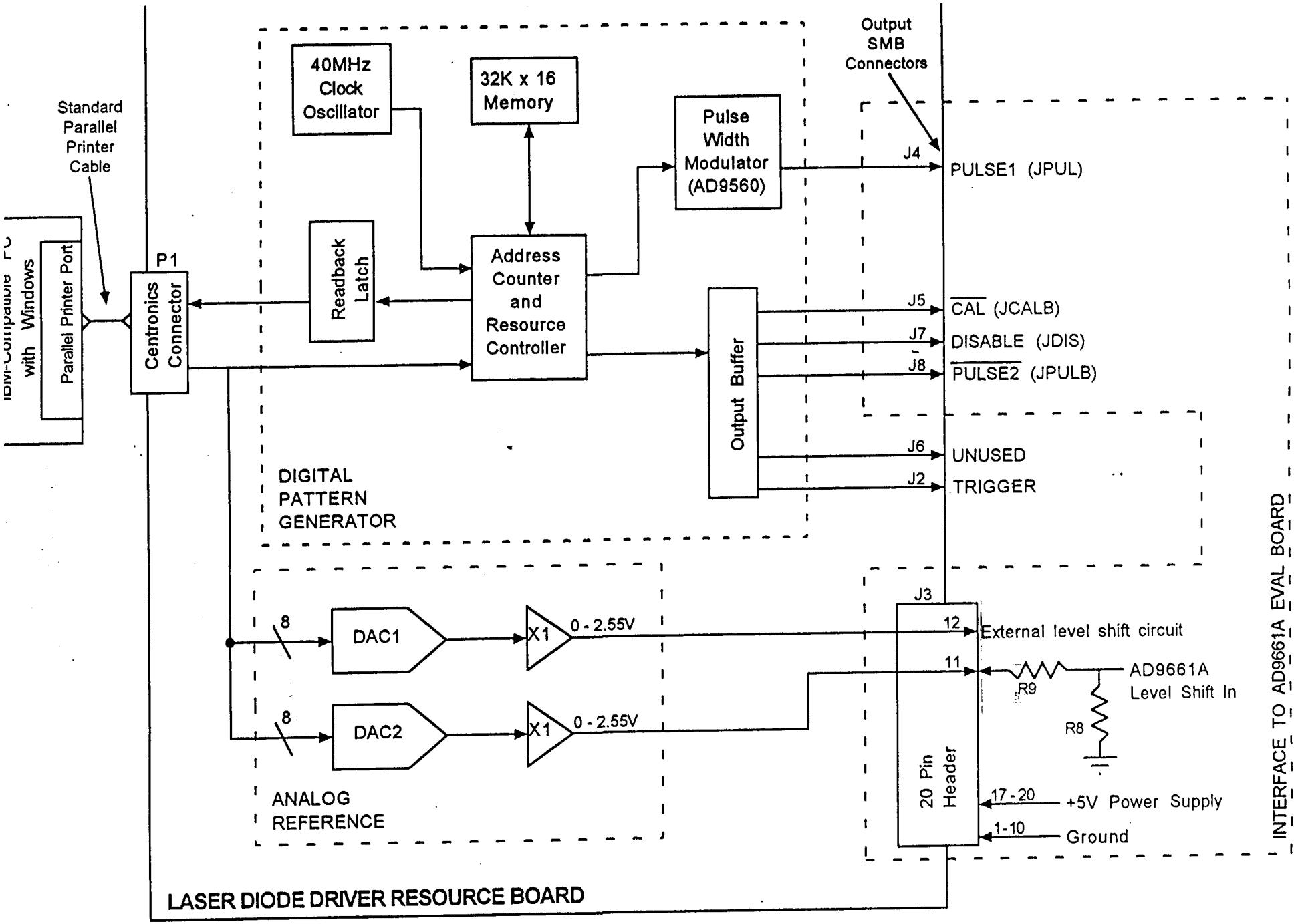
Our mailing address is:

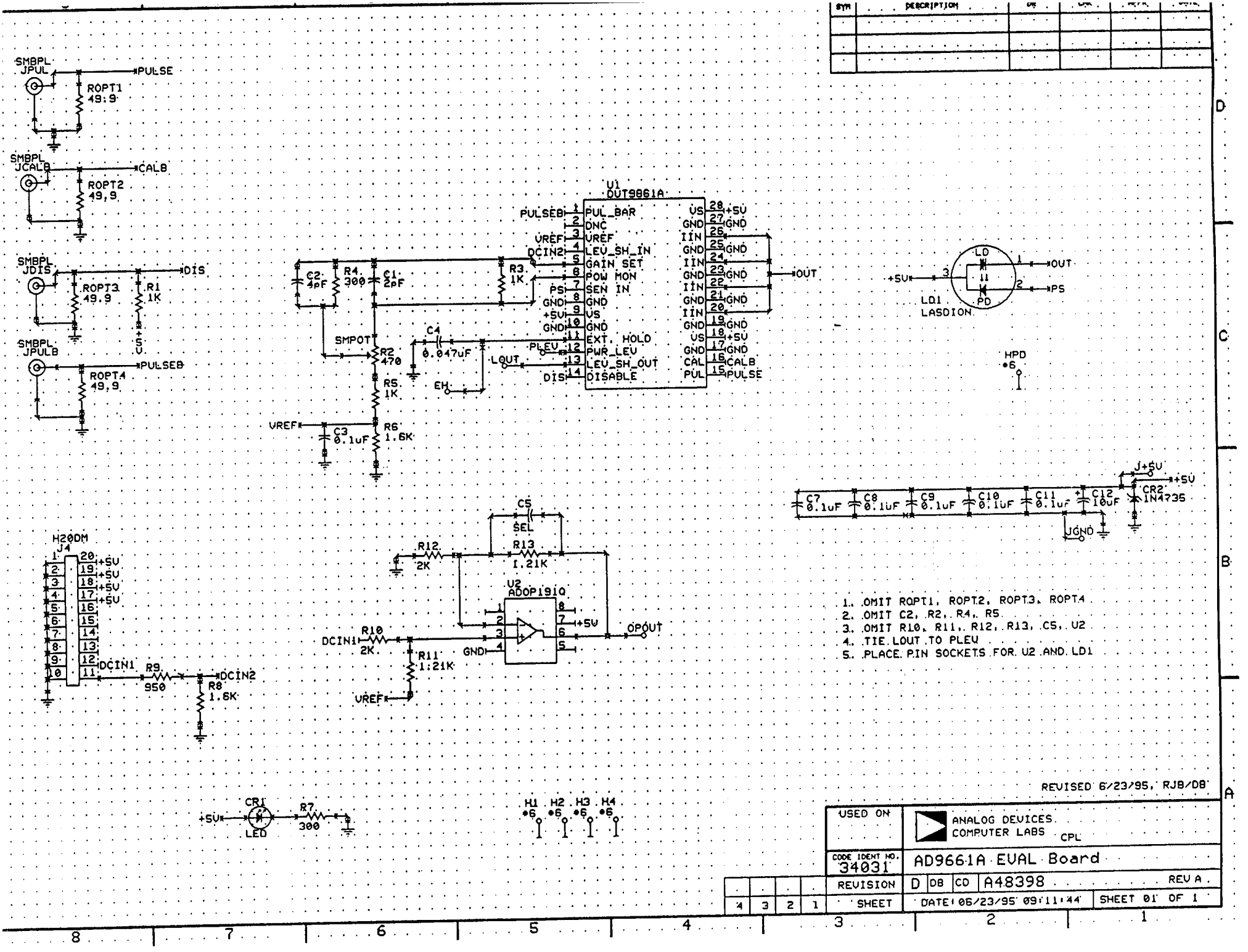
Analog Devices
CPL Team
7910 Triad Center Drive
Greensboro, NC 27409

Attachments:

1. LDD Resource Board Block Diagram
2. SCAN50.61A pattern description
3. SCAN50D.61A pattern description
4. SCANP2D.61A pattern description
5. SCANMIX.61A pattern description
6. SCANCNT.61A pattern description
7. AD9661A Evaluation Board schematic, layout, bill of materials
8. LDD Resource Board schematic, layout, bill of materials

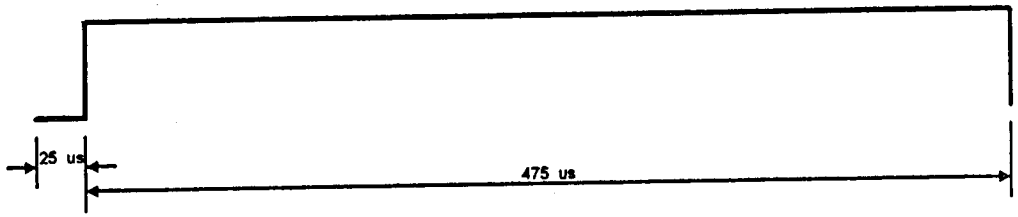
REV 2.0 2/20/96


Standard Parallel Printer Cable
IBM-Compatible PC with Windows
Parallel Printer Port
P1
Centronics Connector
40MHz Clock Oscillator
32K x 16 Memory
Readback Latch
Address Counter and Resource Controller
Pulse Width Modulator (AD9560)
Output Buffer
Output SMB Connectors
J4
PULSE1 (JPUL)
J5
CAL (JCALB)
J7
DISABLE (JDIS)
J8
PULSE2 (JPULB)
J6
UNUSED
J2
TRIGGER
DIGITAL PATTERN GENERATOR
8
DAC1
X1
0 - 2.55V
8
DAC2
X1
0 - 2.55V
ANALOG REFERENCE
J3
12
External level shift circuit
11
R9
R8
AD9661A Level Shift In
20 Pin Header
17 - 20
+5V Power Supply
1-10
Ground
INTERFACE TO AD9661A EVAL BOARD
LASER DIODE DRIVER RESOURCE BOARD

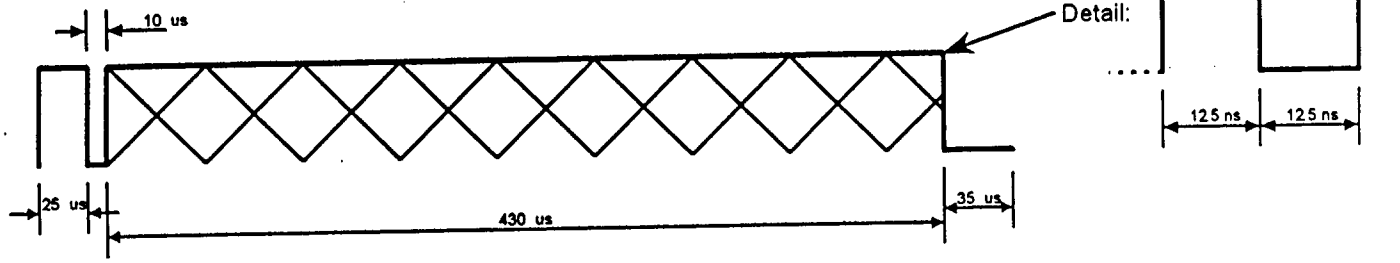

SYM
DESCRIPTION
SMBPL JPUL
PULSE
ROPT1 49.9
SMBPL JCALB
CALB
ROPT2 49.9
SMBPL JDIS
DIS
ROPT3 49.9
R1 1K
+5V
SMBPL JPULB
PULSEB
ROPT4 49.9
U1 DUT9861A
PULSEB 1 PUL_BAR
2 DNC
VREF 3 VREF
DCIN2 4 LEV_SH_IN
5 GAIN SET
8 POW MON
PS 7 SEN IN
GND 8 GND
+5V 9 VS
GND 10 GND
11 EXT. HOLD
PLEV 12 PWR_LEV
LOUT 13 LEV_SH_OUT
DIS 14 DISABLE
VS 28 +5V
GND 27 GND
IIN 26
GND 25 GND
IIN 24
GND 23 GND
IIN 22
GND 21 GND
IIN 20
GND 19 GND
VS 18 +5V
GND 17 GND
CAL 16 CALB
PUL 15 PULSE
OUT
C2 4pF
R4 300
C1 2pF
R3 1K
SMPOT
R2 470
C4 0.047uF
EH
R5 1K
VREF
C3 0.1uF
R6 1.6K
LD
OUT
+5V
PS
LD1 LASDION
PD
HPD
*6
J+5V
+5V
C7 0.1uF
C8 0.1uF
C9 0.1uF
C10 0.1uF
C11 0.1uF
C12 10uF
CR2 IN4735
JGND
H20DM J4
+5V
DCIN1
R9 950
DCIN2
R8 1.6K
C5 SEL
R12 2K
R13 1.21K
U2 ADOP191Q
R10 2K
R11 1.21K
+5V
OPOUT
GND
VREF
1. OMIT ROPT1, ROPT2, ROPT3, ROPT4
2. OMIT C2, R2, R4, R5
3. OMIT R10, R11, R12, R13, C5, U2
4. TIE LOUT TO PLEV
5. PLACE PIN SOCKETS FOR U2 AND LD1
CR1 LED
R7 300
+5V
H1 *6
H2 *6
H3 *6
H4 *6
REVISED 6/23/95, RJB/DB
USED ON
ANALOG DEVICES COMPUTER LABS CPL
CODE IDENT NO. 34031
AD9661A EVAL Board
REVISION D DB CD A48398 REV A
SHEET 4 3 2 1
DATE: 06/23/95 09:11:44
SHEET 01 OF 1
8 7 6 5 4 3 2 1
D C B A

AD9661A Laser Diode Driver Resource Board Pattern Files
Pattern File: SCAN50.61A
Assumptions: CLOCK OSCILLATOR = 40MHz, CHOLD = 0.047uF
Notes: DISABLE always LOW. PWM mode is always Trailing Edge Modulation. Assumes Threshold >25mA.

$\overline{\text{CAL}}$

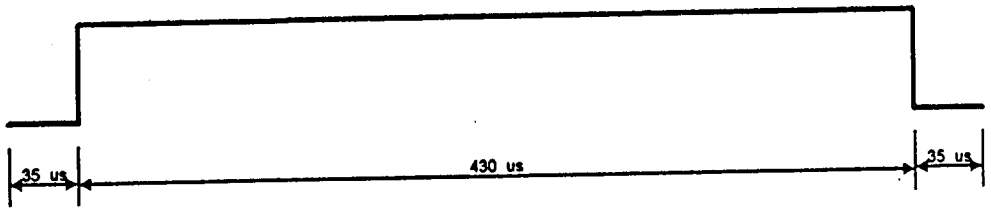


PULSE1



$\overline{\text{PULSE2}}$ always high (inactive)

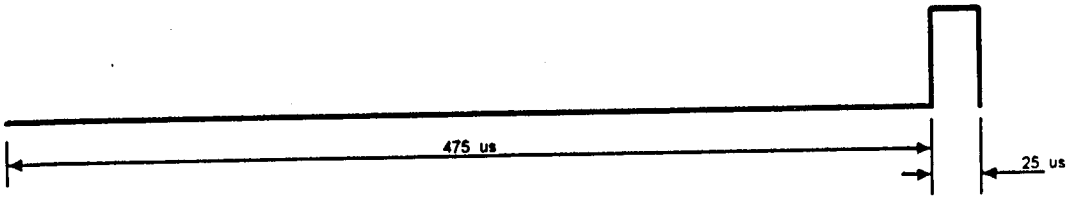
TRIGGER



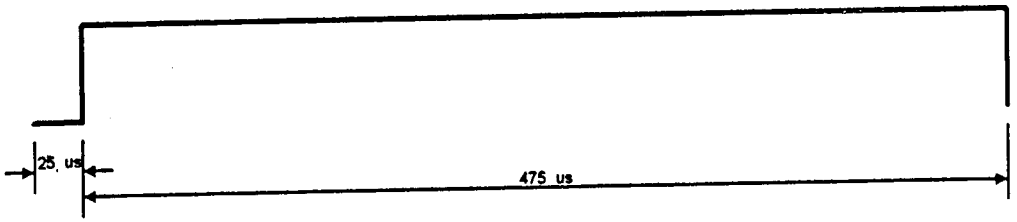
6/22/95

AD9661A Laser Diode Driver Resource Board Pattern Files
Pattern File: SCAN50D.61A
Assumptions: CLOCK OSCILLATOR = 40MHz, CHOLD = 0.047uF
Notes: PWM mode is always Trailing Edge Modulation. Assumes Threshold >25mA.
This pattern demonstrates need for initial calibration.

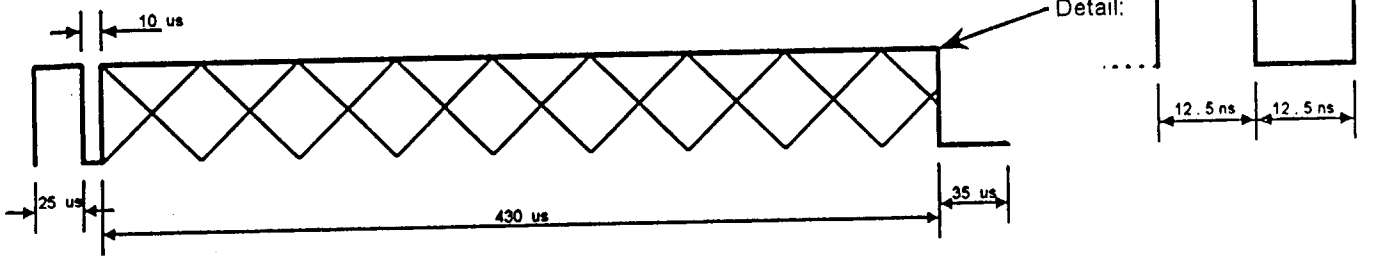
ISABLE



AL

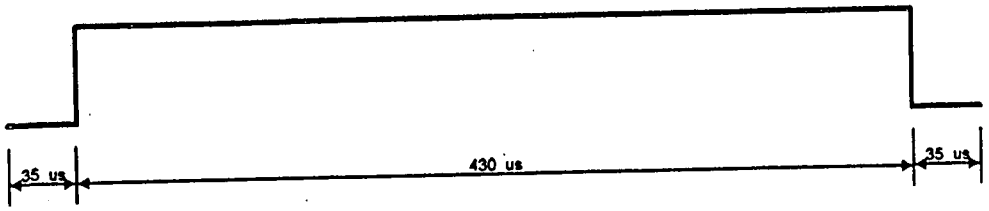


ULSE1



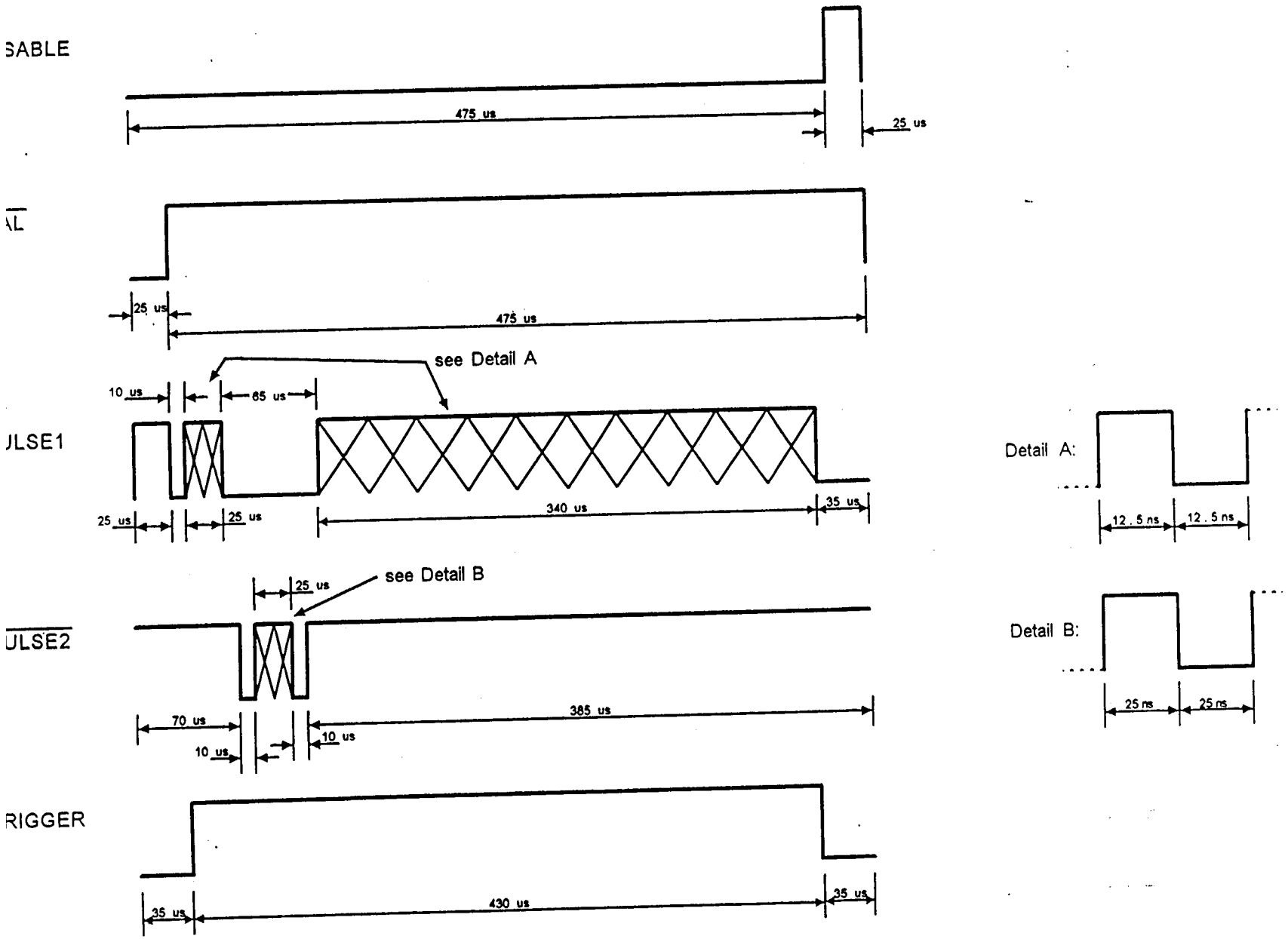
ULSE2 always high (inactive)

RIGGER



6/22/95

)9661A Laser Diode Driver Resource Board Pattern Files
ittern File: SCANP2D.61A
sumptions: CLOCK OSCILLATOR = 40MHz, CHOLD = 0.047uF
otes: PWM mode is always Trailing Edge Modulation. Assumes Threshold >25mA.



3/22/95

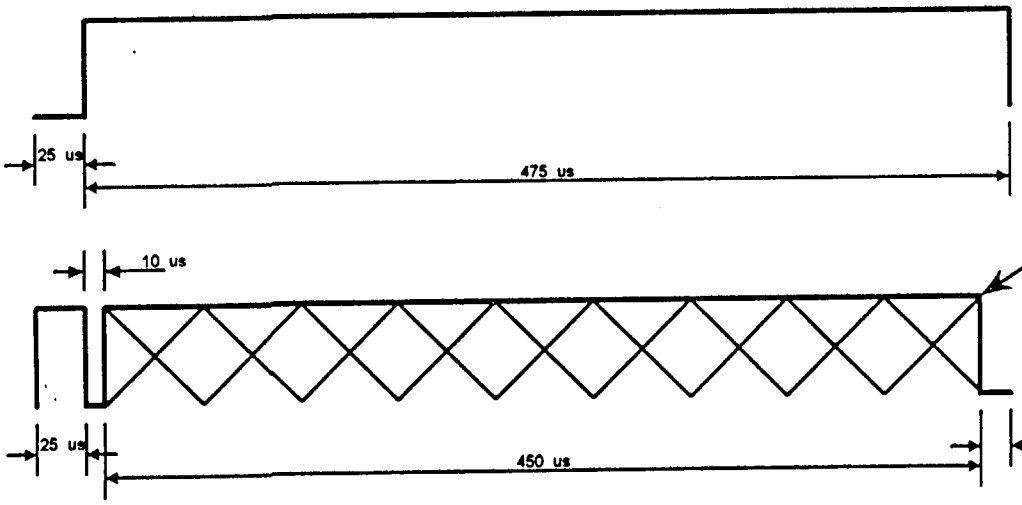
D9661A Laser Diode Driver Resource Board Pattern Files

attern File: SCANMIX.61A

ssumptions: CLOCK OSCILLATOR = 40MHz, CHOLD = 0.047uF

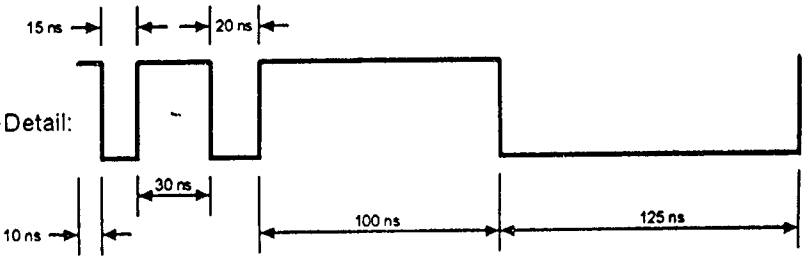
lotes: DISABLE always LOW. PWM mode is always Trailing Edge Modulation. Assumes Threshold >25mA.

:AL



ULSE1

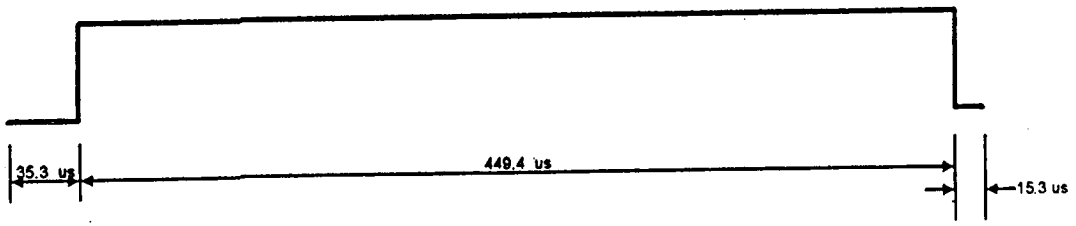
Detail:



Repeat this sequence 1500 times.
1500 x 300ns = 450 us

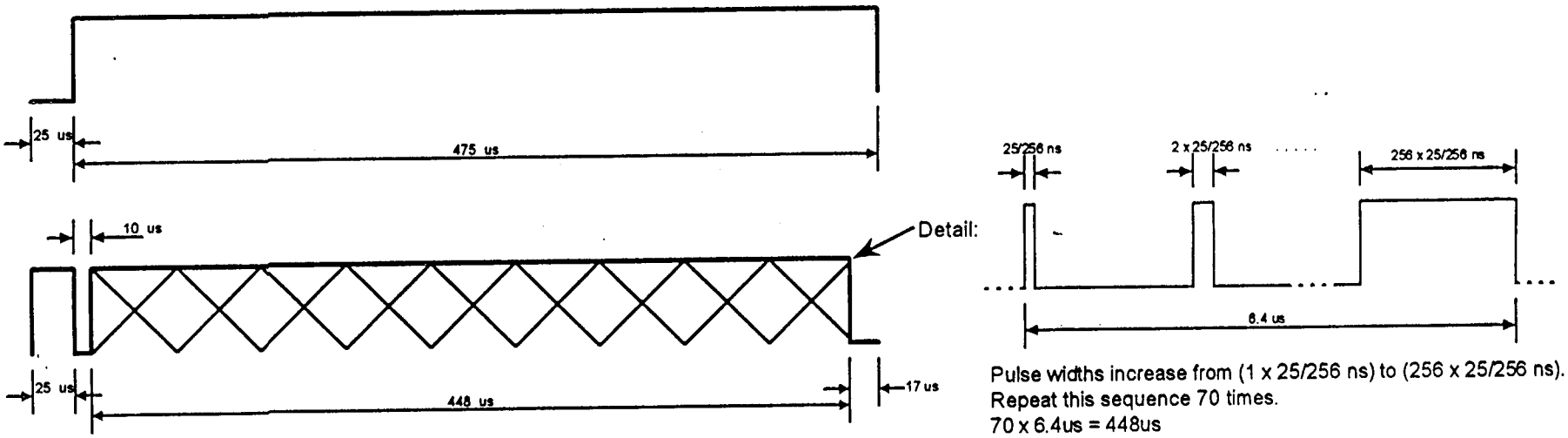
ULSE2 always high (inactive)

RIGGER



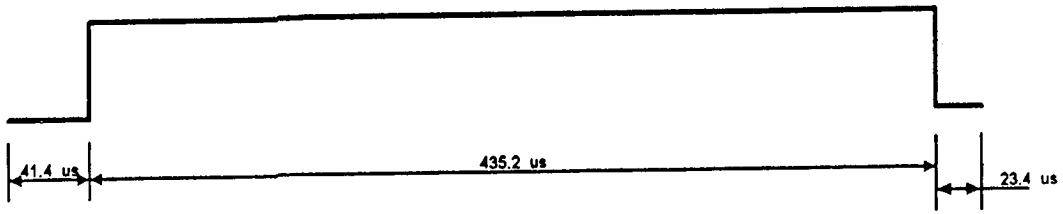
6/22/95

attern File: SCANCNT.61A
ssumptions: CLOCK OSCILLATOR = 40MHz, CHOLD = 0.047uF
lotes: DISABLE always LOW. PWM mode is always Trailing Edge Modulation. Assumes Threshold >25mA.



Pulse widths increase from (1 x 25/256 ns) to (256 x 25/256 ns).
Repeat this sequence 70 times.
70 x 6.4us = 448us

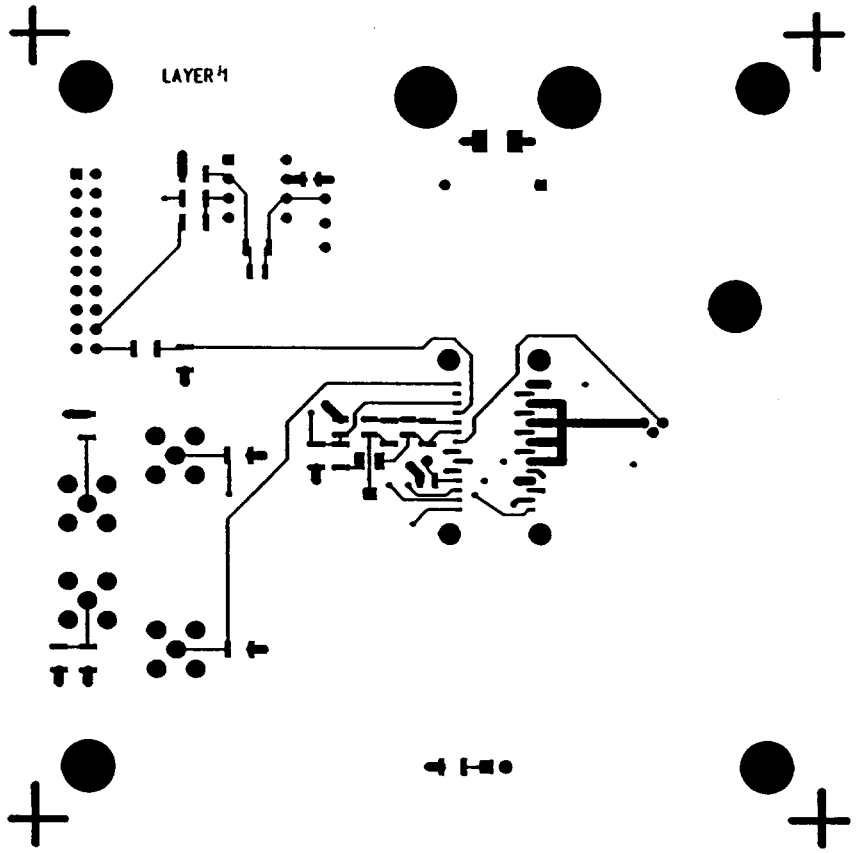
ULSE2 always high (inactive)

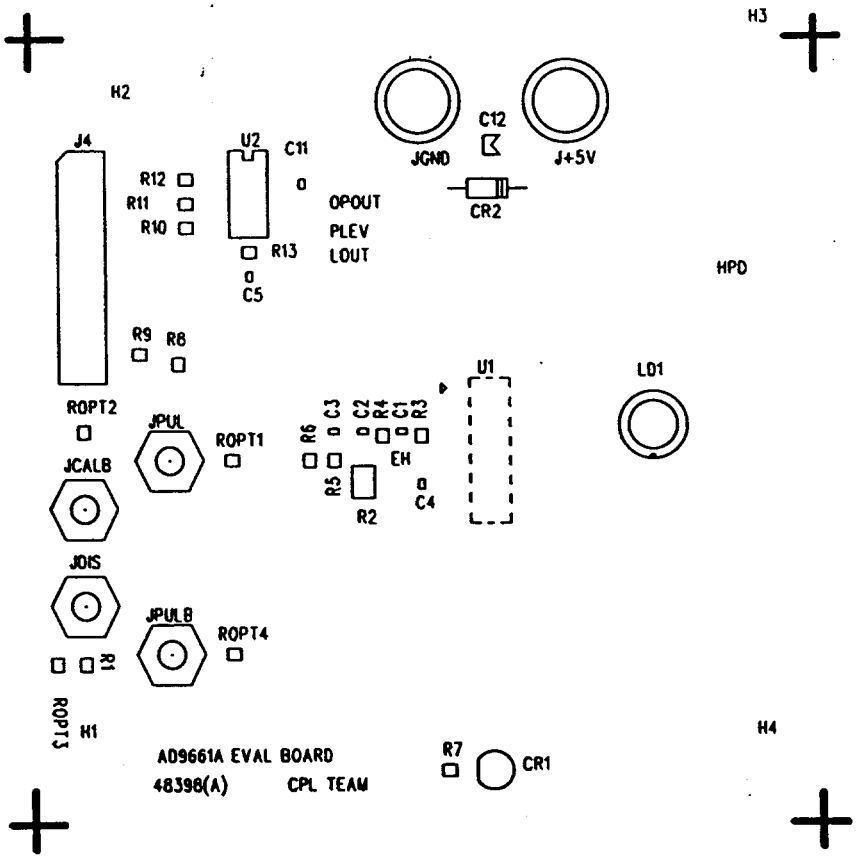


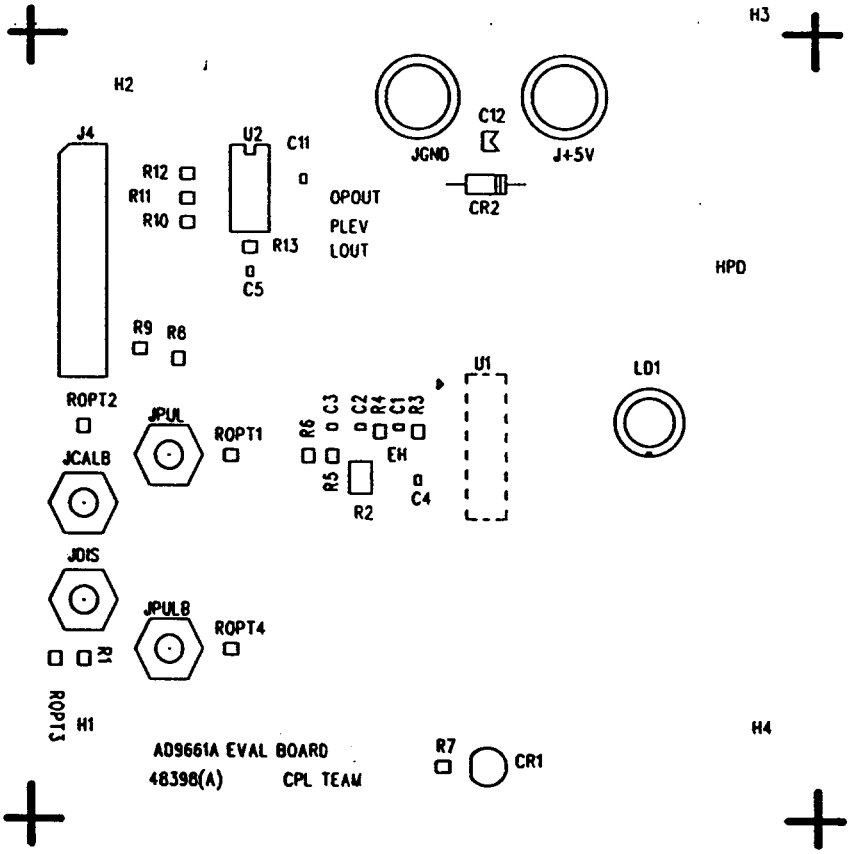
6/22/95

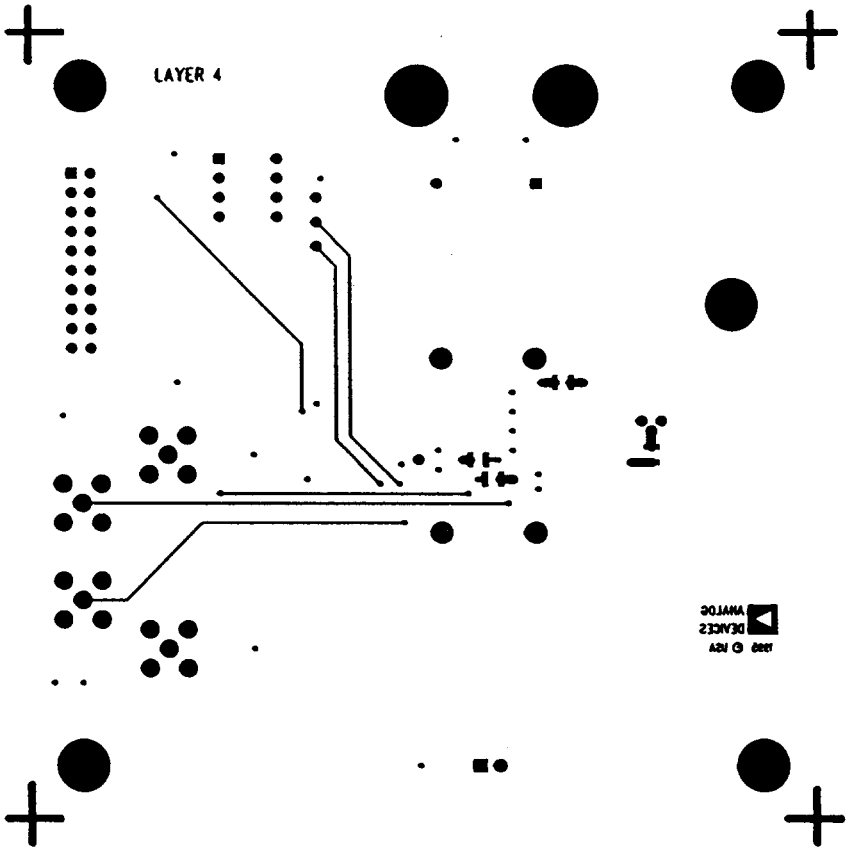
ITEM	QTY	STOCK NO.	REFD	DESCRIPTION
1	1	DUT9661AR -	U1	
2	5		H1,H2 H3,H4 HPD	#6 - #6 SCREW HOLE
3	1		CR2	1N4735 - ZENER DIODE
4	1		U2	ADOP191Q - SING SUP RR I/O OPAMP
5	1		C4	BCAP0805 - CER CHIP CAP 0805,0.047uF,,
6	6		C3,C7 C8,C9 C10, C11	BCAP0805 - CER CHIP CAP 0805,0.1uF,,
7	1		C1	BCAP0805 - CER CHIP CAP 0805,2pF,,
8	1		C2	BCAP0805 - CER CHIP CAP 0805,4pF,,
9	1		C5	BCAP0805 - CER CHIP CAP 0805,SEL,,
10	1		C12	BCAPTAJC - CHIP TANT CAP,10uF,,,
11	2		J+5V JGND	BJACK - BANANA JACK
12	2		R11, R13	BRES1206 - SURF MT RES 1206,1.21K,,,
13	2		R6,R8	BRES1206 - SURF MT RES 1206,1.6K,,,
14	3		R1,R3 R5	BRES1206 - SURF MT RES 1206,1K,,,
15	2		R10, R12	BRES1206 - SURF MT RES 1206,2K,,,
16	2		R4,R7	BRES1206 - SURF MT RES 1206,300,,,
17	4		ROPT1 ROPT2 ROPT3 ROPT4	BRES1206 - SURF MT RES 1206,49.9,,,
18	1		R9	BRES1206 - SURF MT RES 1206,950,,,
19	1	3B08-291	J4	H20DM - HDR 20P DBL ROW MALE

ITEM	QTY	STOCK NO.	REFD	DESCRIPTION
20	1		LD1	LASDION - LASER DIODE (LD: COM ANODE/ PD: COM CATHODE)
21	1		CR1	LED - LIGHT EMITTING DIODE,
22	4		JDIS JPUL JCALB JPULB	SMBPL - SUBMIN SLIDE-ON (MALE) PCB MT PLUG
23	1		R2	SMPOT - SURFACE MOUNT POT ,470
24	4		EH, LOUT PLEV OPOUT	W-HOLE - WIRE HOLE


LAYER 4


H3
H2
J4
U2
C11
C12
JGND
J+5V
CR2
R12
R11
R10
R13
C5
OPOUT
PLEV
LOUT
HPD
R9
R6
U1
LD1
ROPT2
JPUL
ROPT1
C3
C2
R4
C1
R3
R6
R5
R2
EH
C4
JCALB
JDIS
JPULB
ROPT4
R1
ROPT3
H1
AD9661A EVAL BOARD
48398(A)
CPL TEAM
R7
CR1
H4


H3
H2
J4
U2
C11
C12
JGND
J+5V
R12
R11
R10
R13
OPOUT
PLEV
LOUT
CR2
C5
HPD
R9
R8
U1
LD1
ROPT2
JPUL
ROPT1
R6
C3
C2
R4
C1
R3
JCALB
EH
R5
R2
C4
JDIS
JPULB
ROPT4
R1
ROPT3
H1
AD9661A EVAL BOARD
48396(A)
CPL TEAM
R7
CR1
H4


LAYER 4

C10

C8

C3

C1